Cross-Application of Hardware and Software Verification

Po-Chun Chien

SoSy-Lab, LMU Munich

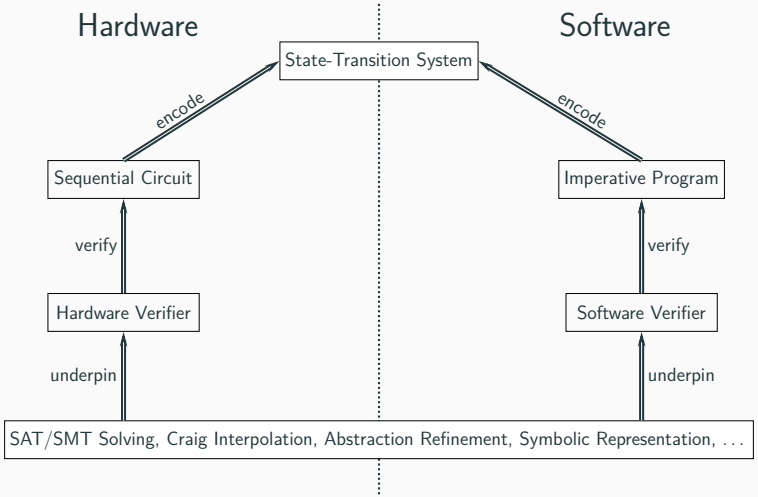
ConVeY Spring Workshop
2024-04-06 @ Luxembourg

SoSy-Lab
Software Systems

LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

ConVeY

Motivation


Hardware
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State-Transition System
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Sequential Circuit
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SAT/SMT Solving, Craig Interpolation, Abstraction Refinement, Symbolic Representation, ...

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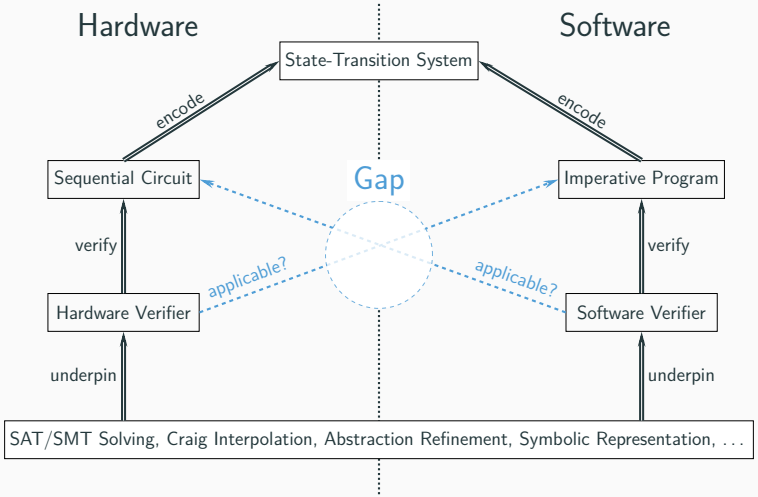
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Briding Hardware and Software Verification

1. Cross-application of HW and SW verifiers

1.1 Applying SW analyzers to HW verification tasks

1.2 Applying HW model checkers to SW verification tasks

2. Knowledge consolidation of HW and SW verification

2.1 Transferring HW algorithms for SW verification

Agenda

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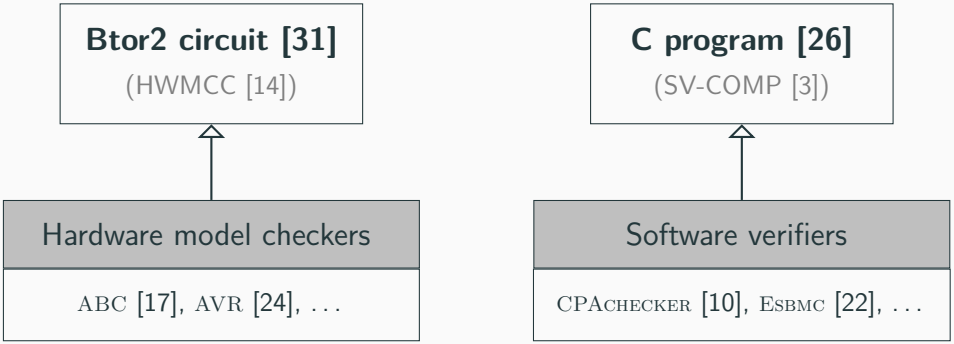

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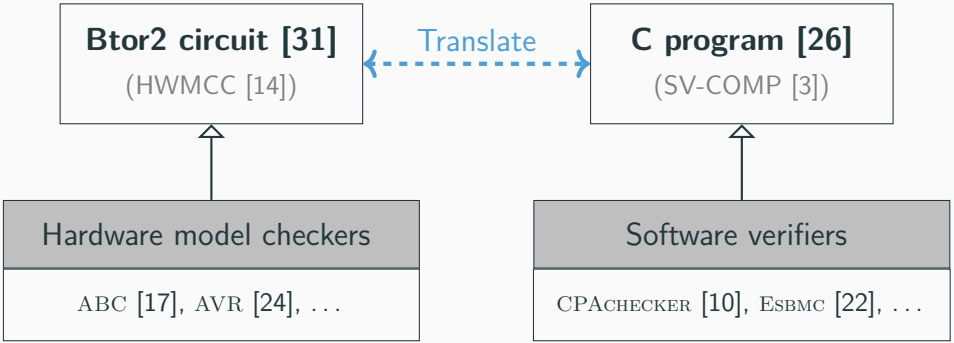

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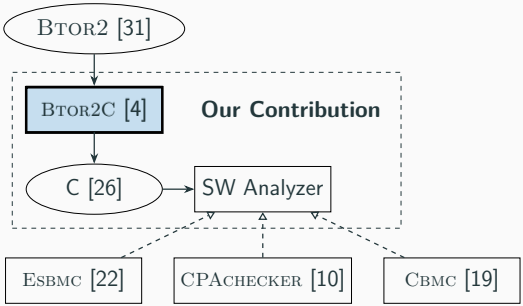
Employing SW Analyzers for HW Verification

- Bridging Hardware and Software Analysis with Btor2C: A Word-Level-Circuit-to-C Translator (TACAS 2023 [4])
- **Btor2-Cert: A Certifying Hardware-Verification Framework Using Software Analyzers (TACAS 2024 [2])**
- Joint work with Zsófia Ádám, Dirk Beyer, Nian-Ze Lee, and Nils Sirrenberg

gitlab.com/sosy-lab/software/btor2-cert

HW-Analysis Tool Chain with Btor2C



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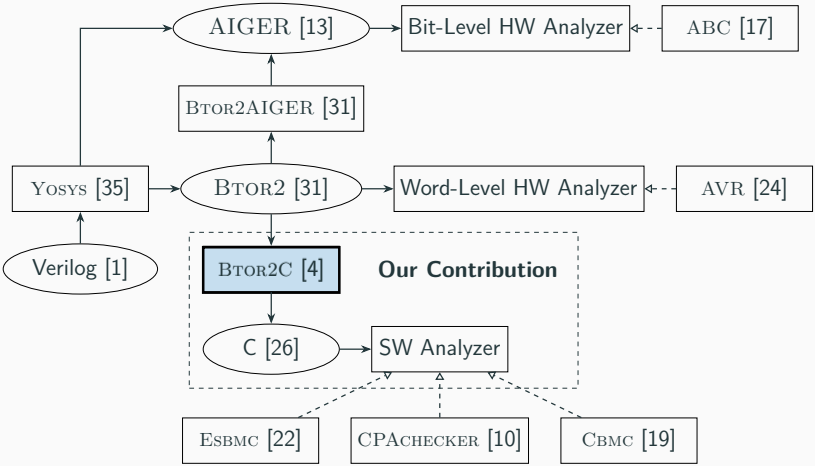

The Btor2 Language

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1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
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7 one 1
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10 ones 1
11 sort bitvec 1
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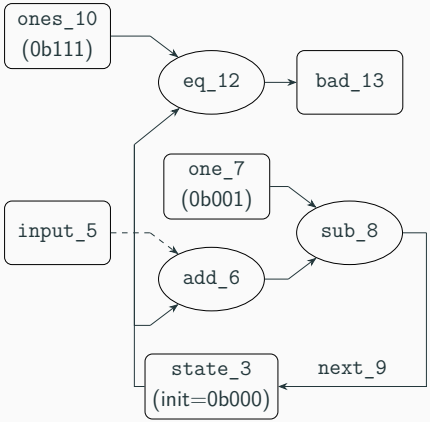

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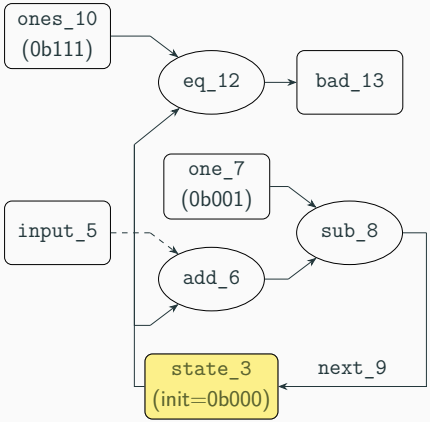

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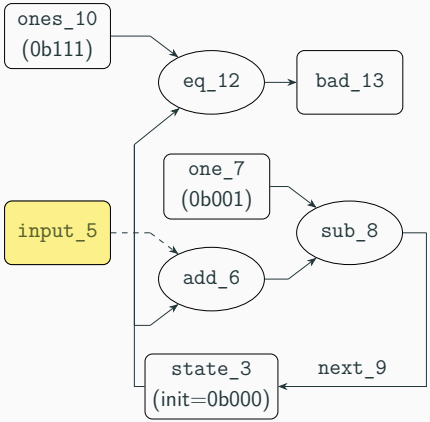

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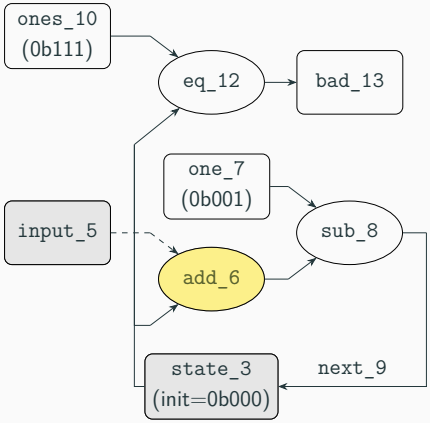

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2    typedef unsigned char SORT_1;
3    typedef unsigned char SORT_11;
4    const SORT_1 var_2 = 0b000;
5    const SORT_1 var_7 = 0b001;
6    const SORT_1 var_10 = 0b111;
7    SORT_1 state_3 = var_2;
8    for (;;) {
9      SORT_1 input_5 = nondet_uchar();
10     input_5 = input_5 & 0b111;
11     SORT_11 var_12 = state_3 == var_10;
12     SORT_11 bad_13 = var_12;
13     if (bad_13) { ERROR: abort(); }
14     SORT_1 var_6 = state_3 + input_5;
15     var_6 = var_6 & 0b111;
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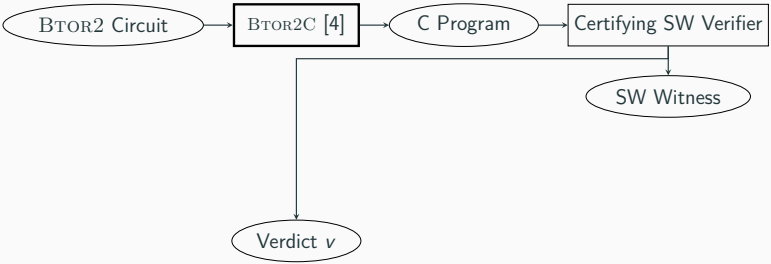
- **RQ1**: How do SW analyzers perform on HW tasks?
  Quite decent! Each analyzer showcases different strength
- **RQ2**: Can SW analyzers complement HW model checkers?
  Yes, **43** tasks were uniquely solved by SW verifiers

Btor2-Cert Framework



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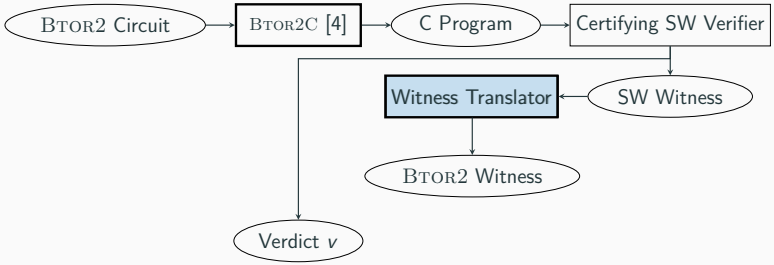

- Translate verification witness: automata [7] to BTOR2 [31]

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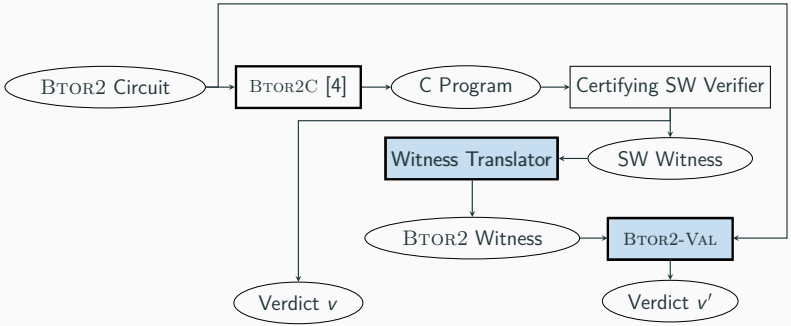

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- BTOR2-VAL: witness validator for BTOR2
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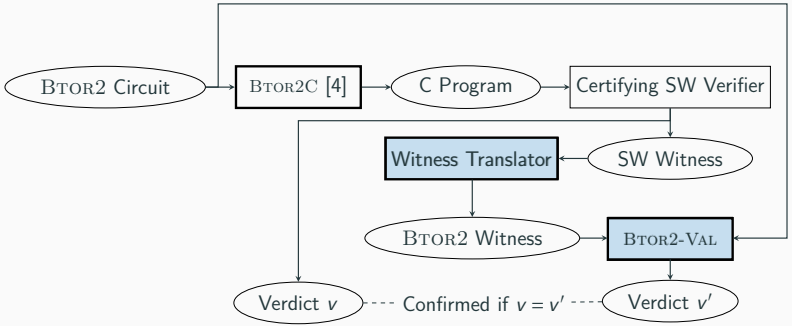

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What Can Btor2-Cert Do for You?

- For HW designers
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- For developers of SW analyzers
  - Validator: witness translation and BTOR2-VAL for performance comparison
  - Verifier: testbed for witness generation
    → Discovery of several bugs in mature software verifiers[1]

[1] `https://www.sosy-lab.org/research/btor2-cert/`

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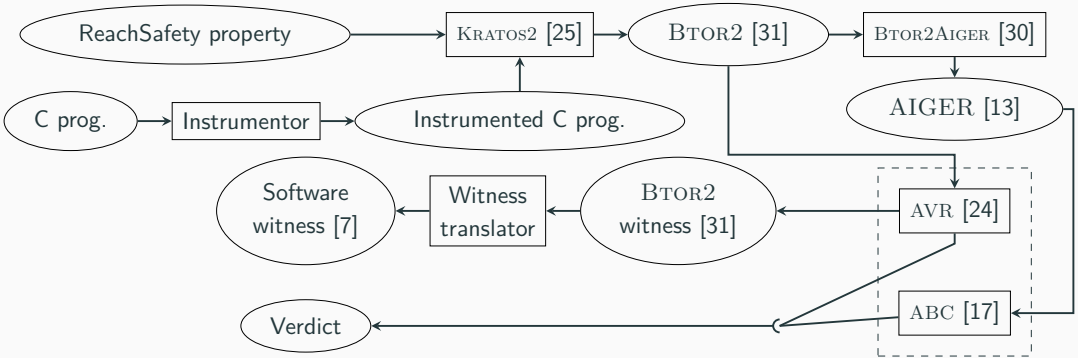
Utlizing HW Model Checkers for Software Verification

- **CPV: A Circuit-Based Program Verifier**
  (SV-COMP 2024 [18])
- Joint work with Dirk Beyer and Nian-Ze Lee

gitlab.com/sosy-lab/
software/cpv

System Architecure



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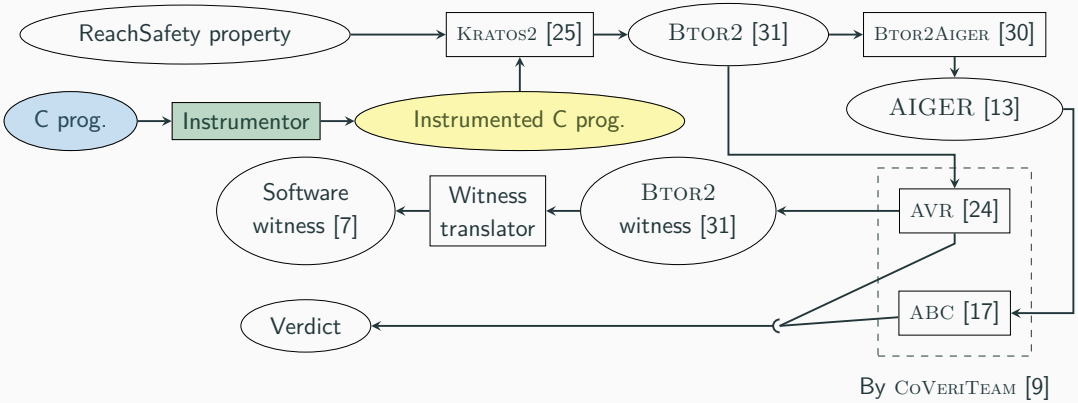
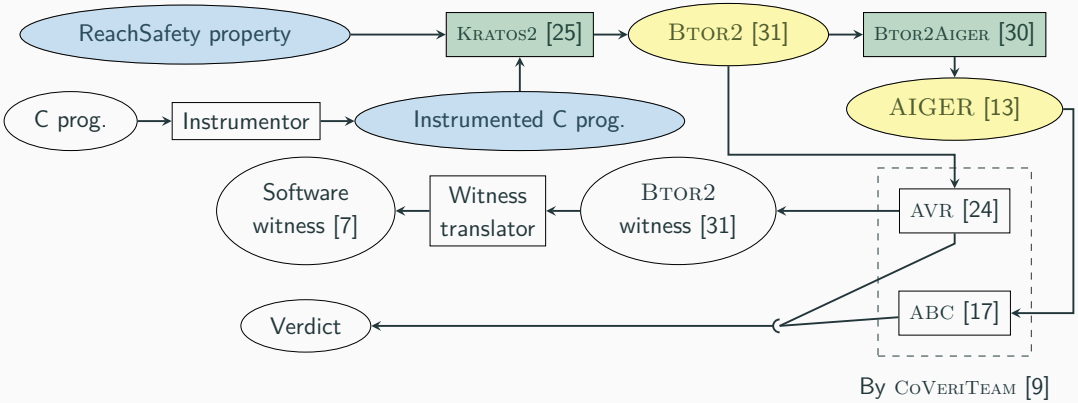


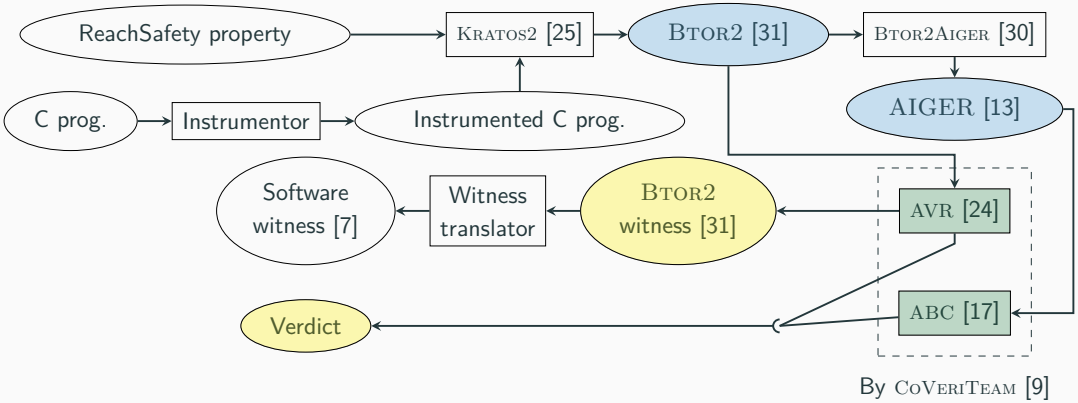
1. Instrument the input program

System Architecure



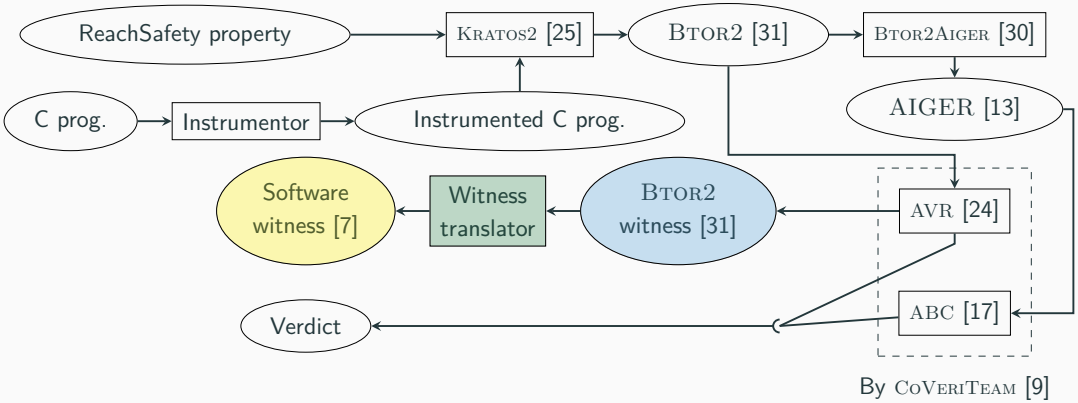
2. Translate the program to a circuit

System Architecure



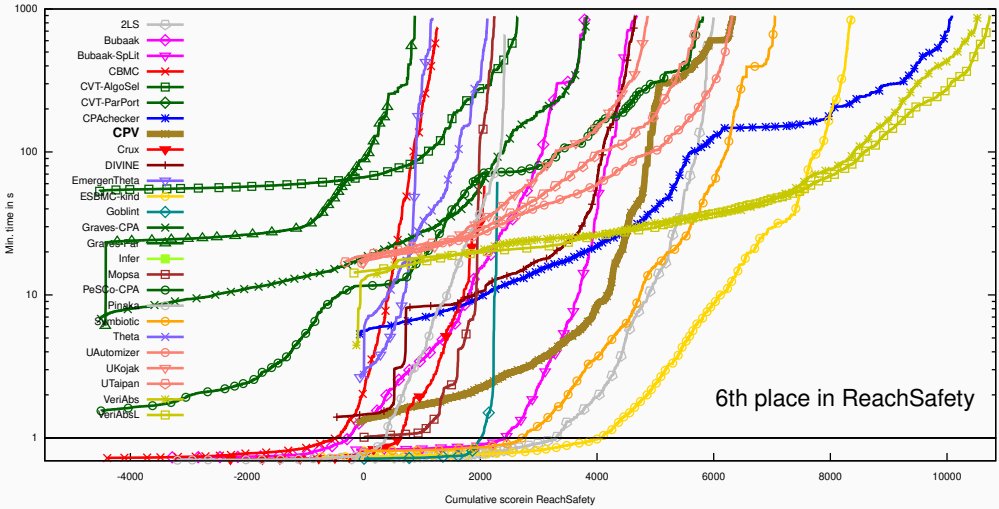
3. Verify the translated circuit with hardware model checkers

System Architecure



4. Translate the Btor2 witness back to software domain

Results in SV-COMP



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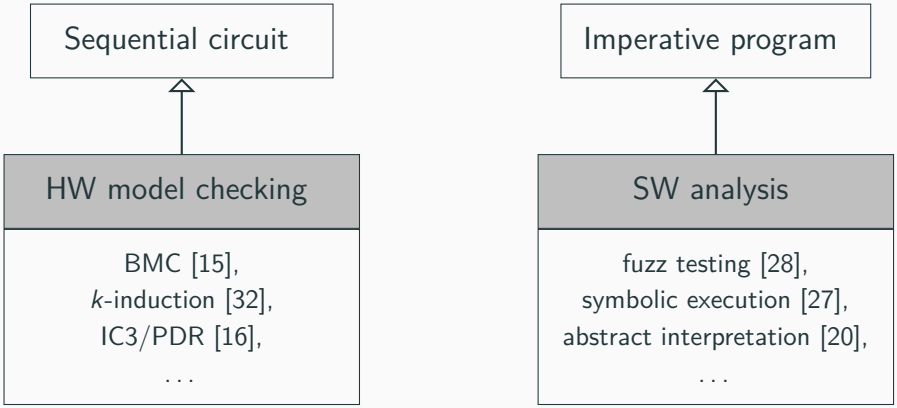
Transferring Verification Techniques Across Domains



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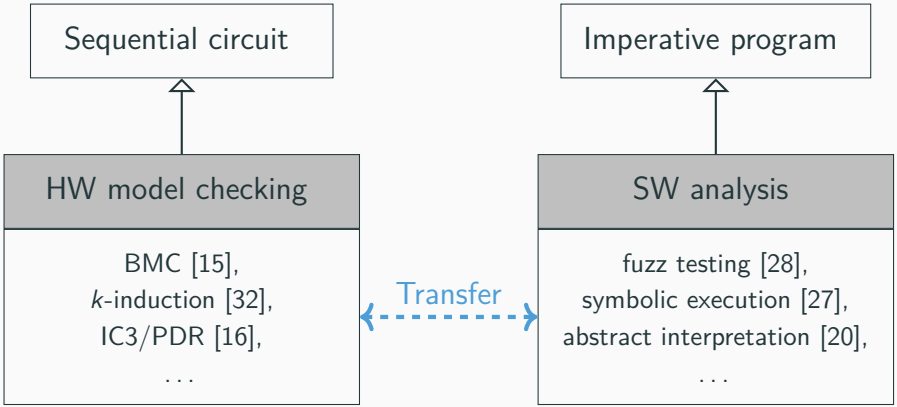

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Transferring HW Model Checking for SW Verifcation

- Interpolation and SAT-Based Model Checking Revisited: Adoption to Software Verification (JAR 2024 [11])
- **Augmenting Interpolation-Based Model Checking with Auxiliary Invariants (SPIN 2024 [6])**
- Joint work with Dirk Beyer, Marek Jankola, Nian-Ze Lee, and Philipp Wendler

www.sosy-lab.org/research/imc-df/

Interpolation-Based HW Model Checking

- HW algorithms implemented in CPAchecker:
  - *Interpolation-Based Model Checking (IMC)* [29]
  - *Interpolation-Sequence-Based Model Checking (ISMC)* [33]
  - *Dual Approximated Reachability (DAR)* [34]

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- Our study shows:
  - Characteristics of these algorithms transferrable
  - These HW algorithms can tackle tasks unsolvable by existing methods
    → cross-disciplinary adoption is beneficial

Augmenting IMC with Auxiliary Invariants

- Strengthen Craig interpolants with auxiliary invariants

Augmenting IMC with Auxiliary Invariants

- Strengthen Craig interpolants with auxiliary invariants
- Augmented vs. plain IMC
  - Improve effectiveness
  - Reduce elapsed wall-time

Conclusion

- Transformation between different representations to leverage their unique strengths

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- Cooperative and cross-disciplinary approaches are beneficial
- Know the state of the art to avoid reinventing the wheel!
- Ultimate goal:
  - HW/SW co-verification
  - Tackle more complex heterogeneous systems

Advertisement

- Try our tools!

Btor2-Cert [2]

CPV [18]

CPAchecker [10]

Advertisement

- Try our tools!

BTOR2-CERT [2]

CPV [18]

CPACHECKER [10]

- **Join our talks at ETAPS!**

COOP:	Sun. 10:30 (more on our work)	SPIN:	Wed. 11:30 (IMC + inv.)
SV-COMP:	Mon. 14:00 (CPV)	TACAS:	Thu. 12:00 (BTOR2-CERT)

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[1] IEEE standard for Verilog hardware description language (2006). https://doi.org/10.1109/IEEESTD.2006.99495

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